# Compensation of Nonlinearities in ΣΔ Modulators Using Digital Assisted Analog Electronics Approach

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***Abstract*—This paper presents a Digital Signal Processing (DSP) technique to compensate nonlinearities in reconfigurable Sigma Delta (ΣΔ) Modulator. In order to design digitally enhanced transceiver, a problem of nonlinearities in these modulators should be addressed. The problem arises due to the constituent building block of ΣΔ Modulators i.e. Digital to Analog Converter (DAC). Since DAC is outside the ΣΔ signal path; the nonlinearities are not reduced by over-sampled quantization and shaping. In this paper, the nonlinearity effects of ΣΔ Modulator are captured by simulating the Signal to Noise Ratio (SNR), Signal to Noise and Distortion Ratio (SNDR), and Spurious Free Dynamic Range (SFDR). For correction, the nonlinearity affected samples are passed to a transversal filter where sample-by-sample compensation is done using the simulated ideal response as a reference. The Normalized Least Mean Square (NLMS) algorithm is employed to adjust and update the filter tap-weights. Simulation results show that for a three-tone input to 4-bit first order ΣΔ Modulator, the SNDR and SFDR improves by 24.6 dB and 34 dB respectively.**

***Index Terms*—ΣΔ modulators, NLMS, nonlinearity, compensation, sigma delta ADC, digital assisted analog circuit, non-linearity correction**

## I. Introduction

Analog to Digital Converters (ADCs) are the basic component that converts the real world analog signals into digital representation. The three basic metrics (speed, resolution and bandwidth) are normally used to characterize the ADCs. Flash ADCs are best suited for high speed applications. However, their resolution is limited to 6~8 bits due to Complementary Metal Oxide Semiconductor (CMOS) process variations [1]. On the other hand, Sigma Delta (ΣΔ) Modulators, based on oversampling and noise shaping principle, are inherently insensitive to CMOS process variations and transistor parameters mismatch. At audio frequencies, their resolution approaches 21~24 bits [2] using a standard CMOS process. Since the process anomalies are increasing with CMOS scaling, these modulators are the natural choice for future high speed designs.

New generation wireless transceivers require high speed, moderate resolution and high bandwidth. The demands of new generation radios require the use of cascaded reconfigurable ΣΔ Modulators that can handle GSM, WCDMA and WLAN standards [3]. For next generation wireless transceivers, the evolving technology of Cognitive Radio/Software Defined Ratio (CR/SDR) requires multi-band antenna, multi-mode RF front-end, multi-standard ADCs, Digital to Analog Converters (DACs) and reconfigurable Digital Signal Processing (DSP). To meet these demanding requirements of multi-standard ADCs/DACs, the ΣΔ technique has become the technology of choice due to its robustness to CMOS process variations, low power dissipation and high design reusability [4].

ΣΔ Modulators have many merits, however, their performance degrades at high Oversampling Ratio (OSR) due to nonlinearity of the constituting building blocks. The basic blocks (summer, flash ADC, integrator, and DAC) of these modulators are inherently nonlinear to a certain extent but the ΣΔ loop lowers the magnitude of nonlinearity in a similar fashion as it reduces and shapes the quantization noise. Since the DAC is outside this compensation loop, its nonlinearity is not reduced; thus making DAC the most critical component, especially in GHz range, that decides the overall performance of the modulator.

Nonlinearity compensation techniques usually incorporate the correction in the feedback loop where it is also affected by the CMOS process variations and mismatches; undermining its effectiveness once the technology shrinks toward nanometer scale. This approach also consumes additional chip area and power. In this paper, compensation technique based on Normalized Least Mean Square (NLMS) algorithm has been proposed to digitally compensate the nonlinearities

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in ΣΔ Modulators. This technique, (programmed in baseband processor not the digital part of ΣΔ Modulators), neither consumes the chip area of the modulator nor depends on specific CMOS technology. It is suitable for modulators that are manufactured in different technology nodes and does not require redesign or calibration effort.

This paper is divided into five sections. Section 2 presents the modeling and characterization of DAC nonlinearity. Section 3 describes the nonlinearity correction methodology and procedure to determine the appropriate compensation filter order. The simulation results are presented in section 4. Section 5 concludes the topic and proposes future work.

## II. DAC Nonlinearity Modeling

The ΣΔ Modulators include summer, integrator, ADC and DAC. Nonlinearity of all these blocks appears in the total digitized output of the modulator. However, the combined nonlinearity contribution of summer, integrator and ADC is much smaller as compared to individual nonlinearity contribution of DAC. This is due to the fact that DAC resides outside the compensation loop. Therefore, the overall linearity of the converter is mainly dependent on the linearity of its internal DAC [5]-[6].

The nonlinearity is commonly characterized in terms of Differential/Integral Nonlinearity (DNL/INL). DNL is the difference between an actual step width and the ideal value of one Least Significant Bit (1 LSB) whereas INL is the cumulative effect of DNL.

To model the DAC nonlinearity, a controlled randomly distributed offset, assuming normal distribution with zero mean and variance σ, has been added to the DAC quantized levels. For one run of the simulation, a specific value of σ adds static DNL errors to the DAC transfer curve. Simulations, for three different cases i.e. (a) Nonlinear ADC only, (b) Nonlinear DAC only (c) Nonlinear ADC and DAC, are carried out to quantize the effect of nonlinearity of the individual components on the cumulative performance of first order 4-bit ΣΔ Modulator.

### A. Non-Ideal ADC

In this case, only 4-bit ADC is nonlinear. For an OSR <=256, the Signal to Noise Ratio (SNR) is degraded by approximately 17dB for an ideal to the worst case.

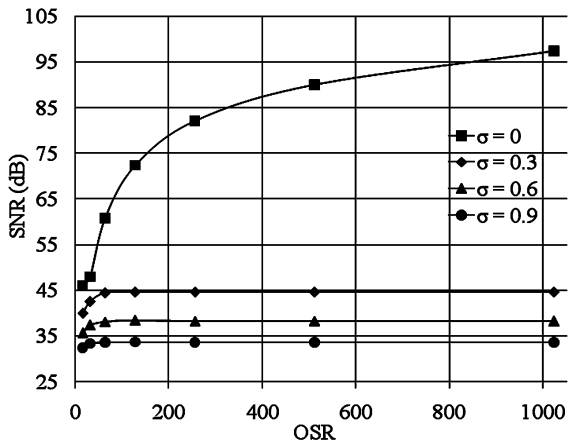



Figure 1. SNR curves for non-ideal DAC.

### B. Non-Ideal DAC

In this case, only 4-bit DAC is nonlinear. For an OSR <=256, the SNR is degraded by approximately 52dB from an ideal to worst case as shown in Fig. 1.

### C. Non-Ideal ADC and DAC

In this case, both ADC and DAC are nonlinear. The SNR curves are similar to case (b) as shown in Fig. 2. It is obvious that the difference between case (b) and (c) is very small. It is also verified from the simulations that the major part of ADC nonlinearity is compensated by the loop.

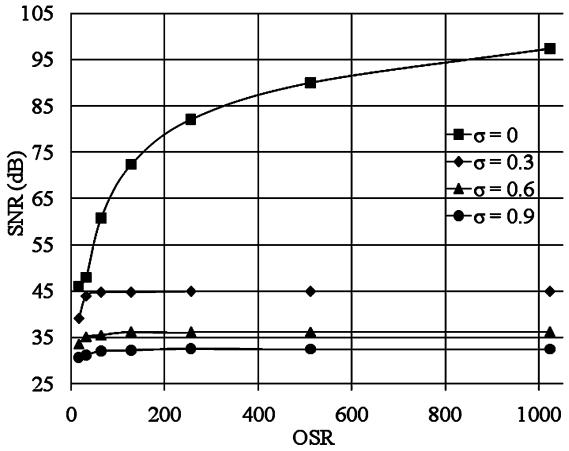



Figure 2. SNR Curves for Non-ideal ADC and DAC.

## III. Correction Methodology

Different techniques are reported to compensate the nonlinearity of the DAC in ΣΔ Modulators. An element trimming is the old and expensive approach. Dynamic Element Matching (DEM) [7]-[8] is a well known technique. It has several variants, including a barrel shifter, Individual Level Averaging (ILA) and Data Weighted Averaging (DWA). However, effective DEM cannot be achieved in case of high resolution feedback DAC [9]-[10]. Reference [11] adopts an approach that uses DSP blocks added right before the DAC in the feedback path and hence this approach has an inherent disadvantage of consuming chip area and increasing the cost.

References [12]-[14] achieve compensation for DAC nonlinearity without consuming chip area in the digital portion of baseband processor, however, this technique requires $2^N$ x K EPROM, where N is the DAC resolution and K represents the bit accuracy of the corrected modulator.

The proposed scheme in this paper differs from already known approaches. The compensation circuitry requirement is fully satisfied by the digital baseband processing power. In this scheme, the baseband processor runs NLMS algorithm to adaptively adjust the weights of compensation filter. Once the weights approach optimum set of values, the nonlinearity present in filter output is significantly reduced.

The proposed technique is inherently all-digital and process independent. It does not consume additional chip

area in the modulator. Moreover, it can be applied to pre-fabricated modulators. The weight adjustment of compensation filter and nonlinearity correction is carried out in two modes called the calibration and normal mode.

### A. Calibration Mode

In this mode, a known stimulus is generated in Matlab™. This stimulus is passed to two modulators. The first one is ideal to generate the desired response whereas the second one depicts the real scenario with nonlinear DAC as shown in Fig. 3. The compensation filter is trained to compensate the DAC nonlinearity by establishing an indirect feedback path to the ideal modulator. The impaired samples are passed to the Linear Transversal Filter (LTF).

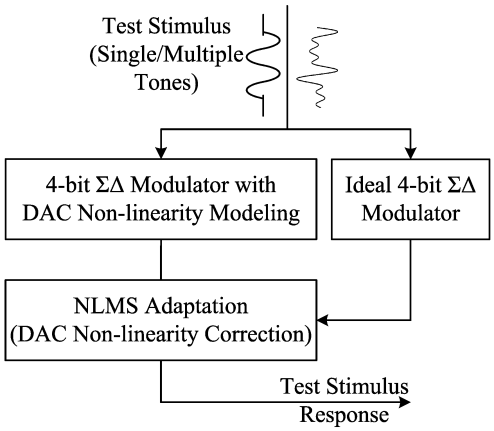



Figure 3. Calibration Mode.

The tap-weight vector is updated by nonlinearity correction algorithm which is based on NLMS adaptation. Since the desired response is known in the form of known test tone response, an error is generated by taking the difference between desired response and the output.

This error is fed to the previous value to update the weights for next iteration. The update of filter weights is stopped once the weights of compensation filter achieve an optimum value. In order to find the filter order, different graphs of SNDR, Spurious Free Dynamic Range (SFDR) and filter order M for irreducible minimum mean-square error were plotted. For illustrative purposes, μ=0.2 is selected. It is clear from Fig. 4 that the optimal filter order in this case is 5 and increasing the filter order further does not improve the SNDR and SFDR significantly.

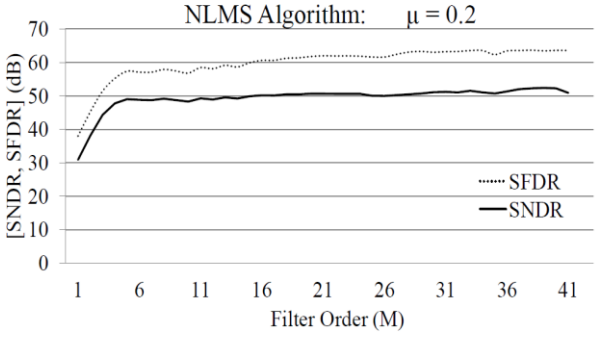



Figure 4. Filter Order Selection

### B. Normal Mode

In this mode, normal stimulus is given to the compensation filter. Since the weights of the compensation filter are adjusted for optimum values, the compensation filter reduces the DNL/INL of the modulator. In this scenario, there is no direct feedback path between modulator and correction filter, however, the weights of the compensation filter were adjusted a priori for known multiple tone stimulus in calibration mode. This pre-adjusted filter tracks the nonlinearities introduced by DAC.

In normal mode, the update of filter coefficients is not required. It is highly unlikely that the coefficient will change as the optimum set of coefficient has already been achieved in calibration mode. The algorithm will allow the update in case it finds the new optimum set better than the previous one.

## IV. Simulation Results

The proposed correction methodology is applied in two scenarios; when the inputs are (a) Single tone and (b) Multiple tones. The first scenario is simple due to the absence of Inter Modulation (IM) products, so the effects of nonlinearity are not well pronounced. In case of multiple tones, IM products simulate a realistic scenario.

Single and multiple tone samples are injected into the modulator. For a single tone, $f_{IN}$ = 5MHz, whereas for multiple tones, $f_{IN1}$ = 3MHz, $f_{IN2}$ = 5MHz and $f_{IN3}$ = 7MHz are generated. The typical OSR of 256 is selected for this simulation. This value comes from the popular real world scenario of IEEE 802.11b, where signal frequency is 2.4GHz. This frequency is reused as sampling frequency and requires an OSR of 240 to digitize 10MHz bandwidth [12]. These multiple tones, at different baseband frequencies, are passed to the oversampling modulator where a controlled nonlinearity is added in the DAC model. These impaired samples are passed to the LTF that has already been adjusted, in calibration mode, for optimum convergence set under NLMS adaptation algorithm.

### A. Single Tone Testing

In this case, an oversimplified scenario has been simulated using single tone as a test signal. For a DNL value of ±0.2 LSB, SNDR is degraded from 82.2dB to 42.6dB. This degradation is compensated by an NLMS algorithm for μ = 1 which improves it to 63.1dB. Similarly, SFDR is degraded from 94.1dB to 49.8dB and corresponding improvement of 24.6dB has been achieved. The degradation and improvement plots of SNDR and SFDR are shown in Fig. 5.

### B. Multiple Tones Testing

In this case, multiple tones are injected as test signal. This case presents a more realistic scenario due to the presence of a large number of IM products. For a DNL value of ±0.2 LSB, SNDR degrades by 40.4dB whereas SNR and SFDR are degraded by 35.9dB and 46.2dB respectively. The degradation in these parameters is compensated by the NLMS algorithm for μ = 1. The

SNDR, SNR and SFDR are improved by 28.5dB, 24.9dB and 34.6dB respectively as shown in Fig. 6.

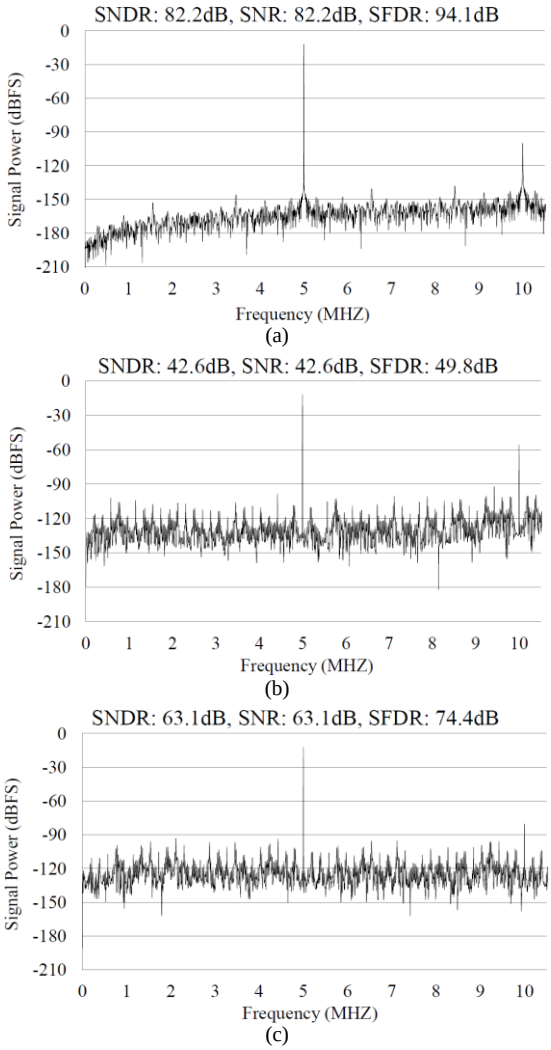
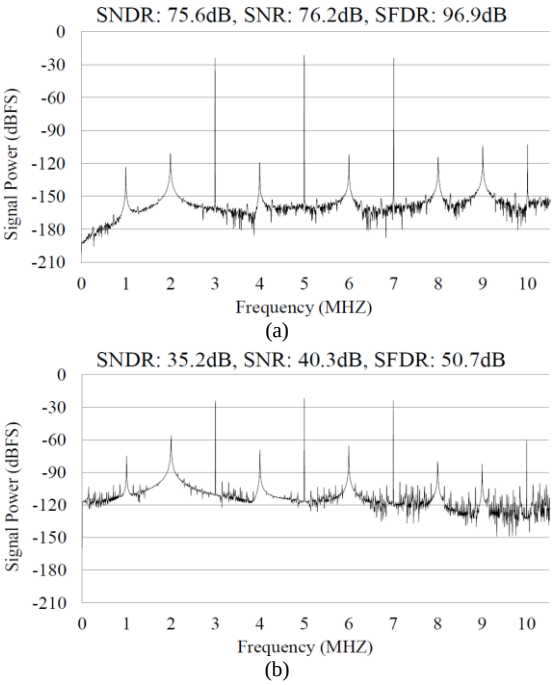



Figure 5. Single Tone (a) Ideal (b) Nonlinear (c) Corrected



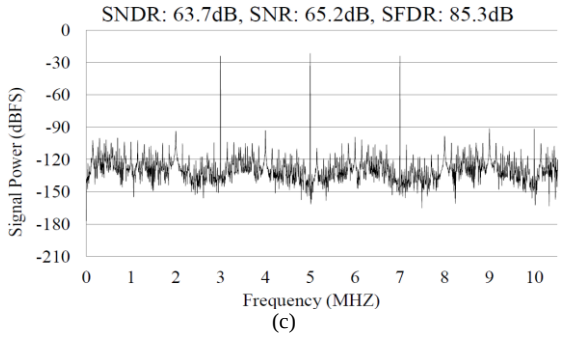




Figure 6. Multiple Tones (a) Ideal (b) Nonlinear (c) Corrected

## V. Conclusion

In this paper, a technique to combat the nonlinearities of ΣΔ modulators is presented. This scheme uses the baseband processing power instead of additional hardware in analog or digital domain of the modulator. Simulation results, for first order high OSR 4-bit modulator show the efficacy of the presented scheme and validate the idea.

In future we plan to implement the front-end in silicon and the baseband algorithm in an FPGA to test the algorithm for real world signals. This hardware implementation will give us the exact processing resources required to implement the algorithm. It is obvious that, for a simulation scenario discussed in this paper, the data generated by 4-bit first order ΣΔ modulator with sampling rate of 2.4GS/s can be easily processed using a normal 32 bit baseband processor with clock frequency of 300MHz.

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