Dynamic Noise Margin Analysis of a Low Voltage Swing 8T SRAM Cell for Write Operation

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***Abstract*—This paper presents the analysis of dynamic noise margin of proposed 8T static random access memory (SRAM) cell. The proposed SRAM cell has two voltage sources, one connected to the bit line and the other is connected to bitbar line. These voltage sources are used to reduce the swing voltage at the output nodes. This reduction of swing voltage causes the reduction in dynamic power dissipation of the proposed SRAM cell during switching activity. The dynamic noise margin (DNM) analysis is carried out and the results are compared with those of conventional 6T SRAM cell and existing 10T SRAM cell for different word line pulse widths. The proposed SRAM cell has higher value of DNM which ensures the higher stability than 6T and 10T SRAM cells. Simulation has been done in 65nm environment with a power supply of 1V. Microwind 3.1 is used for simulation purpose.**

***Index Terms*—CMOS, dynamic power, dynamic noise margin, pulse width, sram, voltage swing, word line**

I. Introduction

CMOS SRAM memory plays a critical role in modern VLSI design. Due to its complex 6T structure, SRAM cache is one of the high power consuming components in the system-on chip (SoC) design [1]. As a result, SRAM cell transistors normally use minimum width to length ratios to minimize the area constraint. This is coupled with the increased fluctuations in transistor parameters like threshold voltage and process parameters. This also affects the stability of SRAM cell. Another major concern is the power consumption of high density SRAM. So to increase the stability and to reduce power dissipation problem different SRAM models and techniques have been proposed. In [2], a leakage energy reduction technique in deep submicron cache memory has been proposed. A novel 9T SRAM cell has been proposed in [3]. In [4], a dynamic word line voltage swing for low leakage is shown. In [5], the authors propose an orthogonal approach which is based on the concept of bit line voltage calibration, i.e., the voltage difference sensed by the sense amplifier is calibrated in order to take into account the effect of the bit line leakage current. The calibration process, performed by a dedicated circuitry placed at the input of the sense amplifier. The self reverse bias bit line technique is to invert the pre-charging value of the bit line so as to force a low-leakage state on the un-accessed cells [6]. In floating bit line strategy [7], the authors propose a design technique that allows bit line floating by turning off the pre-charging transistors. The leakage current from the bit cells automatically biases the bit line to a mid rail voltage that reduces the bit line leakage current. Negative word line, has been shown in [8] that successfully cuts off the bit line leakage by applying negative voltage to inactive word lines. A word line under-drive, in fact, imposes a negative gate-to-source voltage on the access transistors, which in turn show reduced sub-threshold conductance. This method, however, has never been used alone on real SRAMs, because it suffers from degradation of device reliability since the oxide of the pass-gate is over-stressed. A number of recent literatures also presents on the static and dynamic stability analyses of 6T, 7T, 8T, 9T SRAM cells for read and write operations [9], [10], [11], [12].

This paper discusses the dynamic noise margin (DNM) analysis of the proposed SRAM cell. The proposed SRAM cell has two voltage sources. These voltage sources reduce the dynamic power dissipation during switching activity and improve the stability of SRAM cell. The proposed SRAM cell has higher dynamic noise margin than the other existing SRAM cells.

The paper is organized as follows: Section II discusses on the conventional SRAM cell. Section III describes circuit design and working principle of the proposed novel 8T SRAM cell. Section IV shows the detail analysis of dynamic noise margin (DNM) of the proposed SRAM cell for read and write operations. A comprehensive simulations results and discussions are

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presented in section V and finally, section VI concludes the paper.

II. Conventional 6T SRAM Cell

Fig. 1 shows the circuit diagram of a conventional 6T SRAM cell. Word line is used for enabling the access transistors TN3 and TN4 for write operations [13]. Bit and bitbar lines are used to store the data and its compliment. For write "1" operation, the bit line is high and the bitbar line is low. For writing "0", the bit line is low and the bitbar line is high. When the word line is asserted high, the transistors TN3 and TN1 are on and any charge stored in the bit line goes through TN3-TN1 path to ground. Due to zero value at Q, the TP2 transistor is ON and TN2 is OFF. So the charge is stored at Q bar line. Similarly during the write "1" operation, due to high bit line and low bitbar line TN4 and TN2 are ON and the charge stored on the Q bar is discharged through the TN4-TN2 path and due to this low value on the Q bar, TP1 is ON and TN1 is OFF, so the charge is stored on the Q.

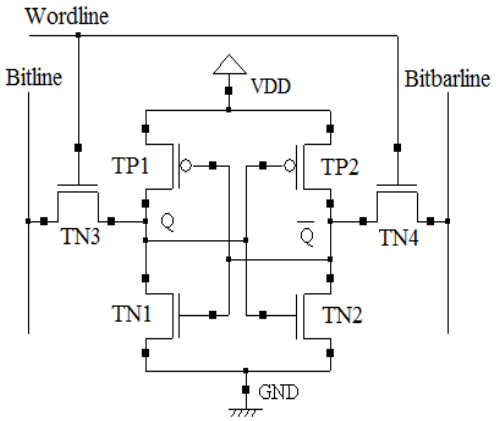

Figure 1. Conventional 6T SRAM cell.

This conventional SRAM cell works on the full swing voltage, so dynamic power dissipation during switching activity from write "0" to write "1" or vice versa, is higher. The similar situation occurs during read operation also.

III. Proposed 8T SRAM Cell

In the proposed design two voltage sources S1 and S2 are connected to the outputs of the bit line and bitbar line. Two NMOS transistors TN5 and TN6 are connected with the inputs of bit and bitbar line directly to switch ON and switch OFF the power supply source during write and read operations. The proposed design has been illustrated in Fig. 2. These power supply sources reduce the swing voltage at the 'out' node when switching activity is being performed.

The dynamic power may be expressed as

$$P_{dynamic} = \alpha C V_{dd} V_{Swing} f \qquad (1)$$

where C = Load capacitance; α = Activity factor; f = Clock frequency; V_{Swing} = Voltage swing at output node.

From (1), it is clear that the dynamic power depends on the swing voltage (V_{Swing}) [14]. This swing voltage is consumed during the switching activity while performing the read/write operations. So, at high speed operation the switching activity also increases and this increases the swing voltage. Increase in swing voltage causes larger dynamic power dissipation at high speed operation.

During the write "0" operation, bit line is low and bitbar line goes high. So the transistor TN6 goes ON and the transistor TN5 goes OFF. Thus the voltage source S2 forces to decrease the voltage swing at the output of the bitbar line. Similarly, when the write "1" operation is performed, TN5 goes ON and TN6 goes OFF, so the voltage source S1 decreases the voltage swing at the output of the bit line. For performing the read operation in the proposed SRAM cell pre-charge circuit and sense amplifier are used. Pre-charge circuits perform the pre-charge operation before the read operation starts. Sense amplifier will produce the voltage difference of the bit and bitbar lines and also amplify the signal during read operation. In the proposed 8T SRAM model voltage sources S1 and S2 reduce the voltage swing and improve the switching activity during write/read operations. These two voltage sources also provide extra voltage during the write/read operations on bit line, bitbar line and word line. This extra voltage also provides less voltage swing for sense amplifier during read operation. Stability is also improved due to better switching capability of the proposed SRAM cell as compared to other SRAM cells.

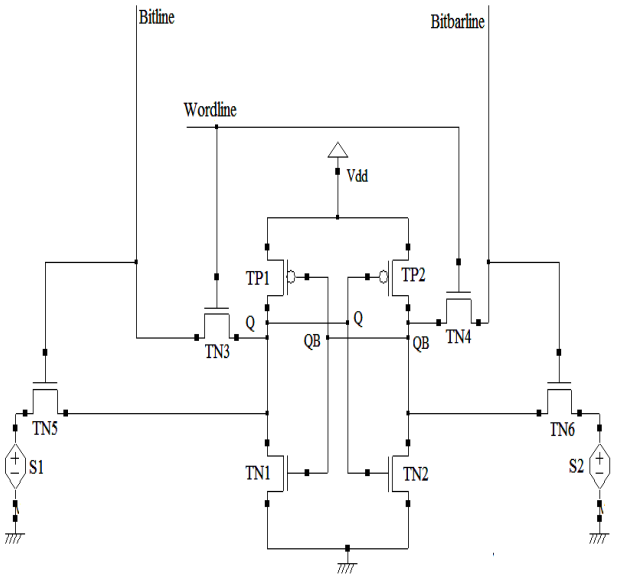

Figure 2. Proposed SRAM cell.

For controlling the noise margin during write/read operations, the sizes of the transistors are a major concern. The rule of thumb is that the width ratio of the transistor TP1 and TN3 is nearly equal to 1.5 and the width ratio for TN3 and TN1 is also equal to 1.5. Similarly, it is applicable for transistors TP2, TN4 and TN2, respectively.

$$\frac{W_{N3}}{W_{P1}} \approx \frac{W_{N1}}{W_{N3}} \approx 1.5 \text{ and } \frac{W_{N4}}{W_{P2}} \approx \frac{W_{N2}}{W_{N4}} \approx 1.5$$

This size configuration provides the proper driving voltage to transistors for ON and OFF conditions.

IV. Write Dynamic Noise Margin Analysis

This section introduces the write DNM approach for measuring stability of the proposed SRAM cell. To define the DNM, the first concern is about the criterion for a write failure. A write failure occurs when the write time is larger than the word line pulse width. The word line pulse width depends on a number of factors, such as the number of bit line and the word line drivers. Write time is defined as the time when the node storing '1' is pulled down from V_{DD} to a critical low value. This write failure definition is valid for most reasonable write cycles. Analysis of the DNM for logic gates has shown that both noise amplitude and noise duration are critical for dynamic stability [15].

DNM is larger than SNM because larger amplitude noise event can be tolerated if it persists for a sufficiently short time. Dynamic stability analysis has been applied to the SRAM cell that has resulted in an analytical model for evaluating its DNM while in the standby mode. This model assumes that the noise source is a current noise pulse injected into the node storing '0'. For a given noise amplitude, the model estimates the critical pulse width, i.e., the minimum pulse duration for the noise to flip the cell's state. A dynamic instability occurs when the injected noise causes the cell's state to follow a trajectory that crosses the boundary of attraction regions [16]. It is assumed that the boundary between attraction regions, also called the separatrix, is always the line where $Q = \overline{Q}$, so this has used the final condition that the two nodes reach to the same voltage. In fact, the assumption about the location of the separatrix is only true for a balanced nominal cell.

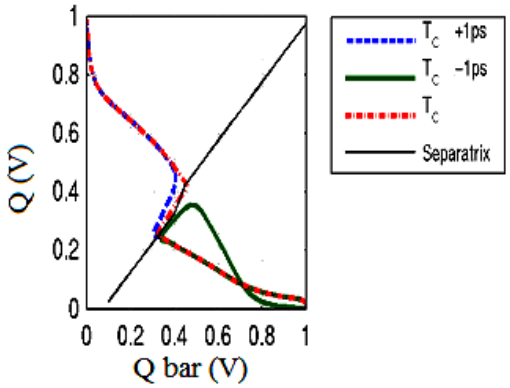

Figure 3. Trajectory for write "1" operation.

In order to evaluate the write ability of a cell more precisely, a metric which takes into account the dynamic write behaviour must be used. On a successful write, Q and Q bar cross over and eventually settle at V_{DD} and 0V, respectively. The word line pulse width (T_{wl}) determines whether or not the two waveforms cross and the write is successful. In this paper it is proposed to use the minimum word line pulse width (T_c) for the cell to flip ultimately to the correct new state as a metric for dynamic write margin. In order to understand T_c as a useful metric, it is related back to the dynamic stability analysis. Fig. 3 shows the trajectories of Q and $\overline{Q}$ for writing "1"when T_{wl} is equal to T_c–1 ps, T_c, and T_c+1 ps. All trajectories overlap on each other as these approach to the separatrix, but these diverge at that point because the word line pulses end at slightly different times. The two trajectories for $T_{wl} \geq T_c$ then overlap again as these converge to the newly written value, but the trajectory for $T_{wl}<T_c$ falls back to the starting state. This simulation clearly shows that T_c is the word line pulse width that causes the state of the cell ($\overline{Q}$, Q) to cross over the separatrix when the word line drops to 50% of V_{DD}. Note that variation has pushed the separatrix off the line $Q = \overline{Q}$. Process variations will make T_C difficult to predict since both the trajectories of the cell state during the word line pulse and the separatrix of the cell will vary with the device parameters.

V. Results and Discussions

This section provides the simulation detail and the comparison analysis of the proposed SRAM cell. Fig. 4 shows the DNM in Monte-Carlo simulation diagram for the proposed SRAM cell. The simulation has been done between noise margin and minimum word line pulse width time (T_c). The simulation has been done at 500 MHz, 45^0C temperature.

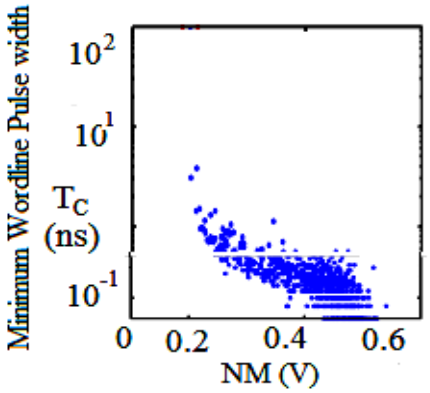

Figure 4. Monte-carlo simulation curve for proposed SRAM cell.

DNM of the proposed SRAM cell is 0.54 V because from Fig. 4 it is evident that the density of blue dots is more in between 0.45 V and 0.6 V. This means that between these voltage values the proposed SRAM cell is more stable. Fig. 5 shows the write "0" and write "1" cycles. Out1 and Out2 signals show the charging and discharging of bit and bitbar lines, respectively. Due to voltage sources S1 and S2 the charging and discharging times for bit and bitbar lines are reduced and this reduction in charging and discharging times reduces the swing voltage that required for switching activity. Reduction in swing voltage causes reduction in dynamic power dissipation. Improvement in switching activity also improves the DNM. Table I shows the variation of DNM with respect to word line pulse width time. From Table I it is evident that when the pulse width time goes from 10

ps to 100 ps the DNM goes down to almost 70% of its original value and after 100 ps as the width time increases, the DNM remains almost constant. At that point DNM saturates and approaches to the SNM value. This has affirmed that the proposed design is more stable compared to the conventional 6T and 10T SRAM cells [17]. The comparison of DNM of 6T, 10T and the proposed 8T SRAM cells has been shown in Fig. 6. Fig. 6 shows that after 100 ps all the SRAM cells go to static condition.

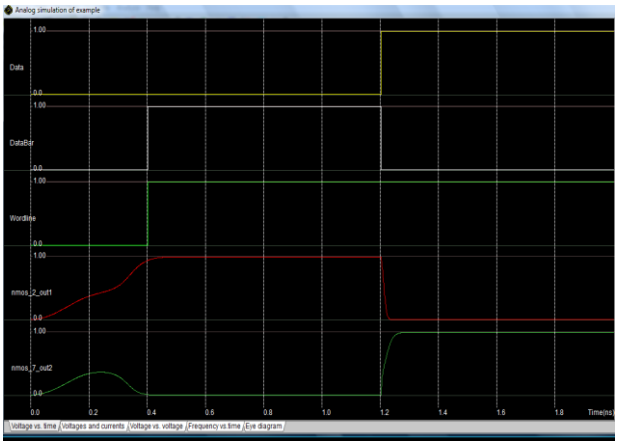

Figure 5. Write cycle of the proposed SRAM cell.

TABLE I. DNM VARIATION WITH NOISE PULSE WIDTH

Word line Pulse Width	Dynamic Noise Margin (mV)		
	Conventional 6T SRAM cell	10T SRAM cell	Proposed SRAM cell
10 ps	820	1460	1712
100 ps	198	390	540
1 ns	197	388	539.4
10 ns	197	388	539.1
100 ns	196.5	387.7	538.8

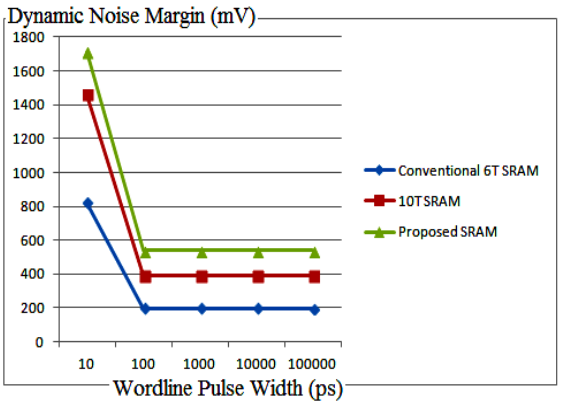

Figure 6. DNM Comparison of SRAM cells.

VI. CONCLUSIONS

To minimize the area constraint, SRAM cell transistors use minimum width to length ratios. But this reduction in width to length ratio increases the power dissipation and reduces the stability of SRAM cell. In this paper a novel design for low dynamic power and highly stable SRAM cell has been proposed. This novel SRAM cell has two voltage sources which are used for reducing the swing voltage during switching activity. The reduction in swing voltage results in reduction of dynamic power dissipation as well as improves the stability of the SRAM cell. This SRAM cell has more dynamic noise margin value than the conventional 6T and 10T SRAM cell. This affirms that the proposed 8T SRAM cell has better stability during dynamic condition. Although number of transistors and area are increased in comparison to conventional 6T SRAM cell but low power dissipation even at very high frequency and higher stability can easily dominate over this drawback. The proposed SRAM cell can be used to provide low power solution in high speed devices like laptops, iPods, mobile phones, electrocardiograms etc.

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